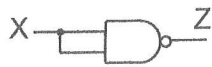


Selected Problem Solutions - Chapter 2

2.1 a)

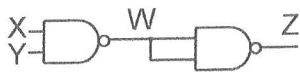


X	Z
0	1
1	0

X	Y	nand
0	0	1
0	1	1
1	0	1
1	1	0

Gate: NOT

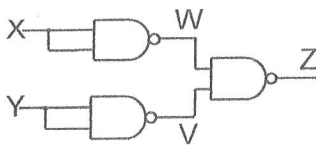
b)



X	Y	W	Z
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Gate: AND

c)



X	Y	W	V	Z
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Gate: OR

2.3

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

$z = x$

$z = \neg x$



$y = 0 \Rightarrow z = x$

$y = 1 \Rightarrow z = \neg x$

2.5

a)  $z = \neg(\neg x \oplus \neg y) = x / y$

x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

x	y	z
T	T	T
T	F	F
F	T	F
F	F	F

0 = TRUE AND gate

b)

 $z = \neg(\neg x \vee \neg y) = x \& y$

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

x	y	z
T	T	T
T	F	F
F	T	F
F	F	F

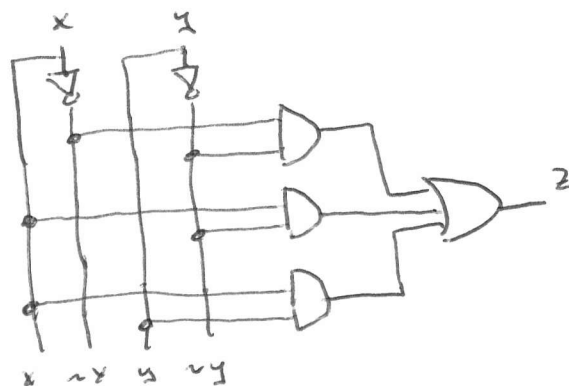
0 = TRUE OR gate

2.7

x	y	z
0	0	1
0	1	0
1	0	1
1	1	1

a) $z = \neg x \& \neg y \vee x \& \neg y \vee x \& y$

b)



c)

$z = x \vee \neg y$

d)



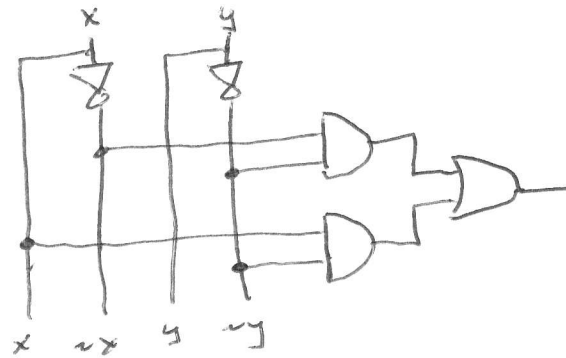
2.9

x	y	z
0	0	1
0	1	0
1	0	1
1	1	0

a)

$$z = \sim x \& \sim y \mid x \& \sim y$$

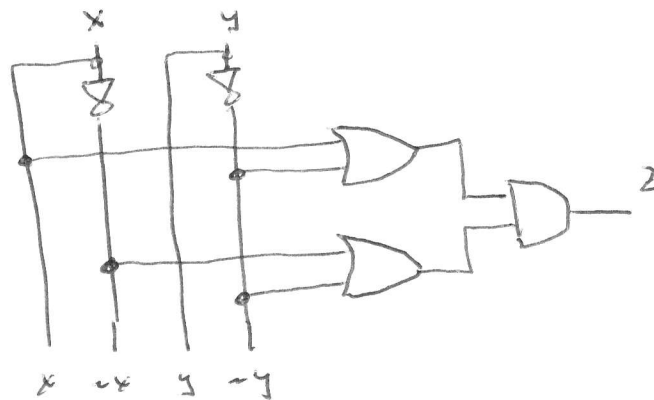
b)



c)

$$z = (x \mid \sim y) \& (\sim x \mid \sim y)$$

d)



2.11

X	$\sim X$	$X \& X$	$X \& \sim X$	$X \mid X$	$X \mid \sim X$	$X \wedge X$	$X \wedge \sim X$
0	1	0 x	0	0 x	1	0	1
1	0	1 x	0	1 x	1	0	1

a) $X \& X = \underline{x}$

b) $X \& \sim X = \underline{0}$

c) $X \mid X = \underline{x}$

d) $X \mid \sim X = \underline{1}$

e) $X \wedge X = \underline{0}$

f) $X \wedge \sim X = \underline{1}$

Problem 2.13

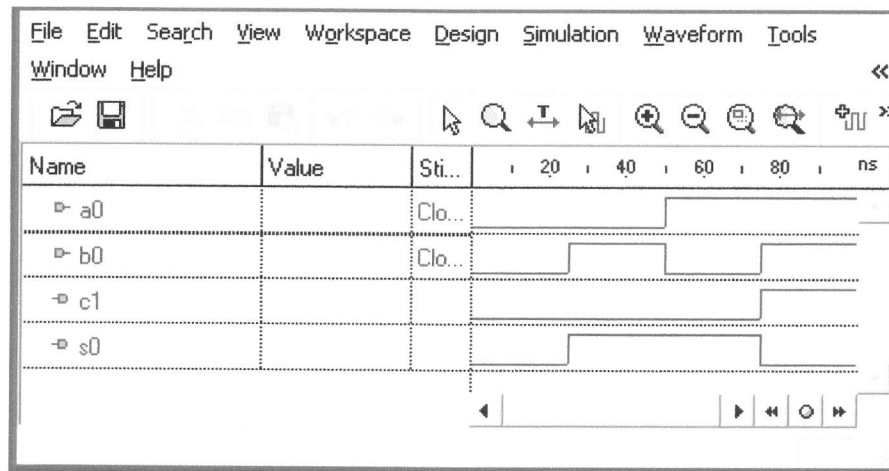
```
-- Title      : P2_13
-- Design     : halfadder
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity P2_13 is
    port(
        a0 : in STD_LOGIC;
        b0 : in STD_LOGIC;
        s0 : out STD_LOGIC;
        c1 : out STD_LOGIC
    );
end P2_13;

architecture P2_13 of P2_13 is
begin

    s0 <= a0 xor b0;
    c1 <= a0 and b0;

end P2_13;
```



a0	b0	s0	c1
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

half adder

Problem 1.15

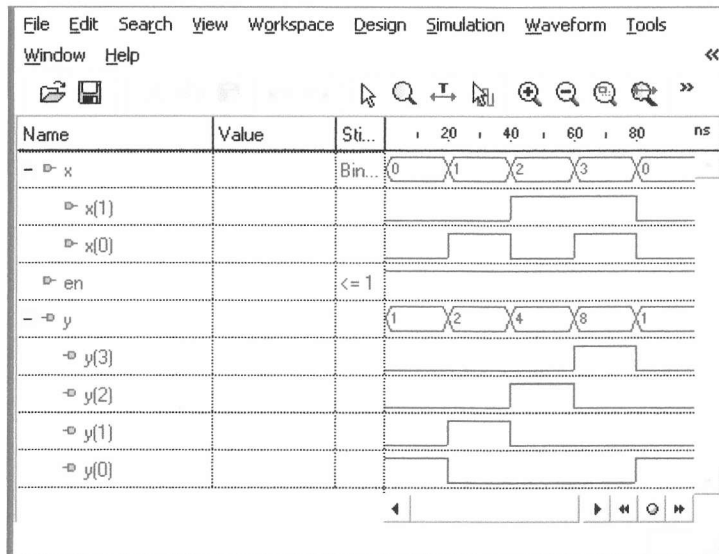
```
-- Title       : P2_15
-- Design      : decode24
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity P2_15 is
    port(
        en : in STD_LOGIC;
        x  : in STD_LOGIC_VECTOR(1 downto 0);
        y  : out STD_LOGIC_VECTOR(3 downto 0)
    );
end P2_15;

architecture P2_15 of P2_15 is
begin

    y(0) <= (not x(1)) and (not x(0)) and en;
    y(1) <= (not x(1)) and x(0) and en;
    y(2) <= x(1) and (not x(0)) and en;
    y(3) <= x(1) and x(0) and en;

end P2_15;
```



$en = 1$

$x(1)$	$x(0)$	$y(3)$	$y(2)$	$y(1)$	$y(0)$
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$y(2) = 1$ when $x(1:0) = 10$